**What Is Claimed Is:**

**1.** A method for integrated processing of different network protocols and multimedia traffics, comprising the steps of:

(a) converting a packet received from a wide area network into a common packet on an external network protocol converter, or converting a packet received from a local area network into a common packet on an internal network protocol converter;

(b) switching said common packet so that said common packet can be switched, bridged, and routed internally;

(c) channelizing to exchange said common packet through dedicated lines according to types of packets;

(d) loading said common packet on a common bus to transmit said common packet to/from a common packet switch; and

(e) identifying a destination address of data and performing an appropriate protocol conversion on a common packet platform, said common packet platform being able to build free topology through an address translation.

**2.** The method of claim 1, wherein said step (a) comprises the steps of:

storing temporarily an external or internal network packet entered in a buffer;

converting said packet into a common packet format; and

loading said common packet on said common bus to transmit said common packet to said common packet switch.

**3.** The method of claim 1, wherein said step (b) comprises the steps of:

storing temporarily said common packet entered in a buffer;

adding a new destination address as desired to a header; and

loading said header on said common packet to transmit said header to the new

destination.

**4.** The method of claim 1, wherein said steps (a), (b), (d) and (e) are modularized so that each of them can be operated independently and they can interwork with one another.

**5.** The method of claim 1, 2, 3, or 4, wherein said steps (a), (b), (d) and (e) constitute a plurality of block combinations according to functions.

**6.** The method of claim 1, 2, 3, or 4, wherein said steps (a), (b), (d) and (e) are integrated on a chip so that they can work as a single chip.

**7.** The method of claim 1, 2, 3 or 4, wherein, in order to support a plug and play function, said steps (a), (b), (d) and (e) are designed as an open architecture and external networks or internal networks interwork with said common packet platform.

**8.** The method of claim 1, wherein, in addition to different network protocol conversions through said step (a), an overlay function toward common packet is supported.

**9.** A system for integrated processing of different network protocols and multimedia traffics, comprising:

a common packet having a header and data to process multi-protocol;

a common packet switch for switching, bridging, and routing said common packet internally;

a plurality of channels for exchanging said common packet through dedicated lines according to types of packets;

a common bus for transmitting said common packet to/from said common packet switch;

a common protocol platform able to build free topology through an address

translation so as to perform integrated processing of different protocols, different packet formats, and so on;

an external network protocol converter for converting a packet received from a wide area network into a common packet; and

an internal network protocol converter for converting a packet received from a local area network into a common packet.

**10.** The system of claim 9, wherein said common packet switch comprises:

a buffer part storing temporarily said common packet entered;

a separate channel part based on types of traffic classes;

a header conversion part where a new destination address as desired is added to a header; and

a loader part loading existing data and said header with said new destination address on said common packet.

**11.** The system of claim 9, wherein said external network protocol converter comprises:

a buffer part storing temporarily an external network packet entered;

a conversion part converting said external network packet into said common packet; and

a loader part loading said common packet on said common bus to transmit said common packet to said common packet switch.

**12.** The system of claim 9, wherein said internal network protocol converter comprises:

a buffer part storing temporarily an internal network packet entered;

a conversion part converting said internal network packet into said common packet; and

a loader part loading said common packet on said common bus to transmit said common packet to said common packet switch.

**13.** The system of claim 9, wherein said common packet, said common bus, said common packet switch, said common packet platform, said external network protocol converter, and said internal network protocol converter are modularized so that each of them can be operated independently and they can interwork with one another.

**14.** The system of claim 9, 10, 11, 12 or 13, wherein said common packet, said common bus, said common packet switch, said common packet platform, said external network protocol converter, and said internal network protocol converter constitute a plurality of block combinations according to functions.

**15.** The system of claim 9, 10, 11, 12 or 13, wherein said common packet, said common bus, said common packet switch, said common packet platform, said external network protocol converter, and said internal network protocol converter are integrated on a chip so that they can work as a single chip.

**16.** The system of claim 9, 10, 11, 12 or 13, wherein in order to support a plug and play function said common packet, said common bus, said common packet switch, said common packet platform, said external network protocol converter, and said internal network protocol converter are designed as an open architecture, and external networks or internal networks interwork with said common packet platform.